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# (54) SEMICONDUCTOR DEVICE AND FORMATION THEREOF

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### (56)References Cited

### U.S. PATENT DOCUMENTS

6,214,679	B1*	4/2001	Murthy H01L 29/41783
			257/E21.165
6,600,200	B1 *	7/2003	Lustig et al 257/371
7,332,439	B2 *	2/2008	Lindert et al 438/696
7,858,481	B2 *	12/2010	Brask H01L 29/42376
			257/224

# (Continued)

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#### (57)ABSTRACT

A semiconductor device and method of forming the same are described. A semiconductor device includes an active area adjacent a gate structure. The gate structure includes a gate electrode over a gate dielectric, the gate dielectric having a bottom surface in a first plane. A second etch interacts with a first composition and an initial dopant to remove a bottom portion of a first sidewall spacer adjacent the gate structure, such that a bottom surface of the first sidewall spacer lies in a second plane different than the first plane. The removal of the bottom portion of the first sidewall spacer reduces a first distance between a source or drain and a bottom surface of the gate electrode, thus reducing proximity loading of the semiconductor device and improving functionality of the semiconductor device.

# 20 Claims, 6 Drawing Sheets

